

CLAIMS

- 1 1. An integrated circuit, comprising:
2 an input port by which data is received from a source external to the integrated
3 circuit;
4 a configurable logic array having a programmable configuration defined by
5 configuration data stored in electrically programmable configuration points within the
6 configurable logic array;
7 memory adapted to store instructions for a mission function for the integrated
8 circuit, to store instructions for an initialization function used to transfer the configuration
9 data to the programmable configuration points within the configurable logic array in
10 response to an initialization event; and
11 a processor coupled to the memory which fetches and executes instructions from
12 the memory.
- 1 2. The integrated circuit of claim 1, including:
2 a programmable configuration memory on the integrated circuit adapted to store
3 the configuration data, wherein said initialization function transfers the configuration data
4 from the programmable configuration memory to the configurable logic array.
- 1 3. The integrated circuit of claim 1, wherein said memory comprises a non-volatile
2 store.
- 1 4. The integrated circuit of claim 1, wherein said memory comprises a floating gate
2 memory store.
- 1 5. The integrated circuit of claim 1, wherein said memory comprises a read-only
2 memory store.
- 1 6. The integrated circuit of claim 1, wherein said memory comprises a first non-
2 volatile store for the initialization function, and a second store for the mission function.

1 7. The integrated circuit of claim 1, wherein said memory comprises a first volatile
2 store for the initialization function, and a second store for the mission function.

1 8. The integrated circuit of claim 1, including a watchdog timer coupled to the
2 processor, and wherein the initialization function includes using the watchdog timer to
3 generate an initialization event in response to errors, and upon the initialization event, re-
4 executing the initialization function.

1 9. The integrated circuit of claim 1, including a watchdog timer coupled to the
2 processor, and wherein the initialization function includes loading the configuration data
3 onto the integrated circuit via the input port on the integrated circuit and using the
4 watchdog timer to generate an initialization event in response to errors, and upon the
5 initialization event, reloading the configuration data via the input port.

1 10. The integrated circuit of claim 1, wherein the initialization function includes
2 receiving encrypted configuration data via the input port on the integrated circuit, and
3 decrypting the configuration data.

1 11. The integrated circuit of claim 1, wherein the initialization function includes
2 receiving compressed configuration data via the input port on the integrated circuit, and
3 decompressing the configuration data.

1 12. The integrated circuit of claim 1, wherein the electrically programmable
2 configuration points comprise non-volatile, charge programmable memory cells.

1 13. The integrated circuit of claim 1, wherein the electrically programmable
2 configuration points comprise nonvolatile, programmable memory cells.

- 1 14. The integrated circuit of claim 1, including:
2 an interface between the processor and the configurable logic array supporting
3 said initialization function.
- 1 15. The integrated circuit of claim 1, wherein said memory stores instructions for an
2 in-circuit programming function to write or modify instructions for the initialization
3 function.
- 1 16. The integrated circuit of claim 1, wherein said memory includes a protected
2 memory array storing instructions for a backup configuration load function, and a second
3 memory array storing instructions for said initialization function, the protected memory
4 array being protected from alteration by an in-circuit programming function and the
5 second memory array being accessible to be written or modified by the in-circuit
6 programming function.
- 1 17. The integrated circuit of claim 1, wherein said processor comprises a configurable
2 logic array configured to execute said instructions.